We claim:

1. An integrated circuit comprising:

a processing core;

an internal memory containing test routines that the processing core executes to test the integrated circuit; and

an interface coupled to the processing core to permit activation of a first output signal indicating a test result from executing the test routines.

2. The integrated circuit of claim 1, wherein the processing core executes the test routines in response to a reset signal.

3. The integrated circuit of claim 2, wherein the interface block comprises:

a first terminal on which the processing core activates the first output signal to indicate the test result; and

a second terminal on which the processing core activates a second output signal to indicate when the first output signal indicates the test result.

4. The integrated circuit of claim 3, wherein the processor toggles the first output signal to verify that the first output signal is functional.

5. The integrated circuit of claim 1, wherein the processing core executes the test routines from the internal memory during a production test of the integrated circuit.

6. The integrated circuit of claim 1, wherein the test routines include tests of the internal memory.

7. The integrated circuit of claim 1, wherein the internal memory contains a first set of test routines for execution during a production test of the integrated circuit and a second set of test routines for execution during an in-product test of the integrated circuit.

8. The integrated circuit of claim 7, wherein a control signal input to the integrated

circuit controls whether the first or second set of routines are executed.

9. A test method for an integrated circuit, comprising:

using a processing core in the integrated circuit to execute test routines stored in the integrated circuit; and

observing a first signal output from the integrated circuit as a result of the processing core executing the test routines, the first signal indicating whether the execution of the test routines detected a failure in the integrated circuit.

10. The test method of claim 9, further comprising observing a second signal output from the integrated circuit, wherein processing core in executing the test routines activates the second signal to indicate when a state of the first signal indicates whether the execution of the test routines detected a test failure.

11. The test method of claim 10, further comprising activating the first signal before activation of the second signal to verify that the first signal is functional.

12. The test method of claim 11, activating an input signal to the integrated circuit to causes the processing core to execute the test routines, wherein activating the first signal before activation of the second signal is in response to the activating of the input signal.

13. The test method of claim 9, observing one or more additional signals from the integrated circuit, wherein the processing core controls the additional signals to indicate a type of failure that executing the test routines detected.

14. The test method of claim 9, wherein the test method is performed during production of the integrated circuit.

15. The test method of claim 14, further comprising controlling an input signal to the integrated circuit to select which of the test routines stored in the integrated circuit are executed.

16. The test method of claim 9, further comprising:

applying a control signal to the integrated circuit; and

selecting the test routines according to the control signal.

17. The test method of claim 16, wherein:

when the control signal has a first state, the test routines selected implement a production test of the integrated circuit; and

when the control signal has a second state, the test routines selected implement a system-level test of the integrated circuit.